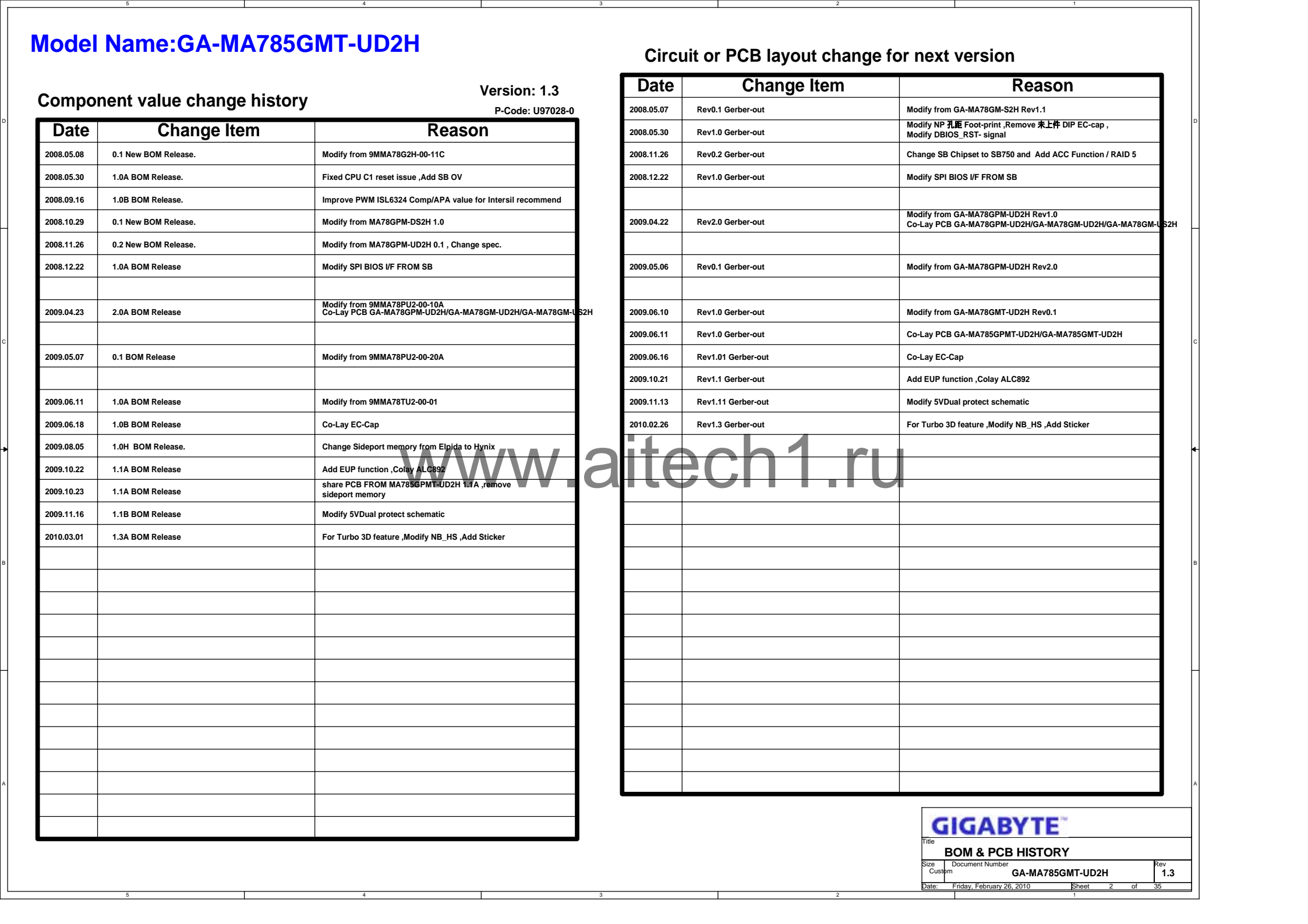
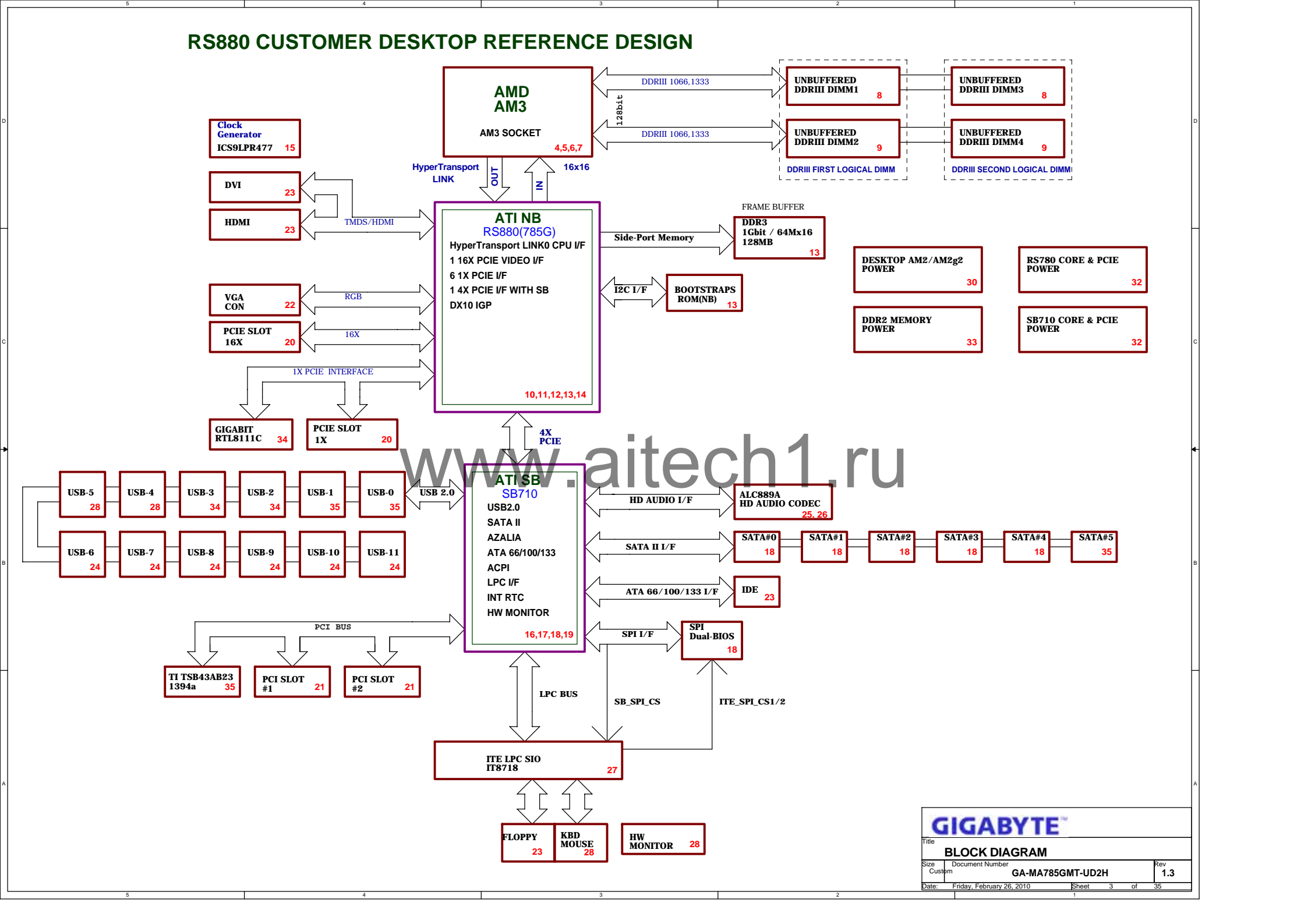
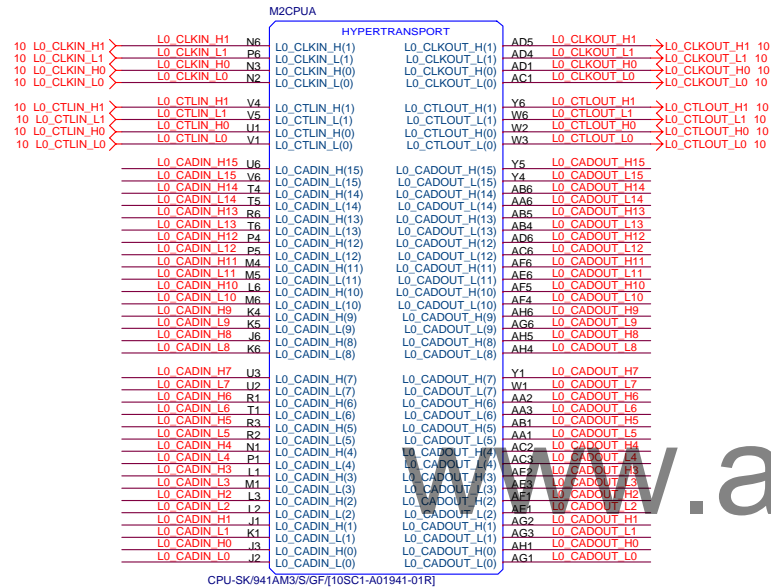


[illegible][illegible][illegible][illegible][illegible][illegible][illegible][illegible][illegible][illegible][illegible]

[illegible]

L0_CADIN_L[0..15] <L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] 10



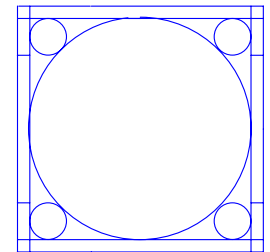
CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

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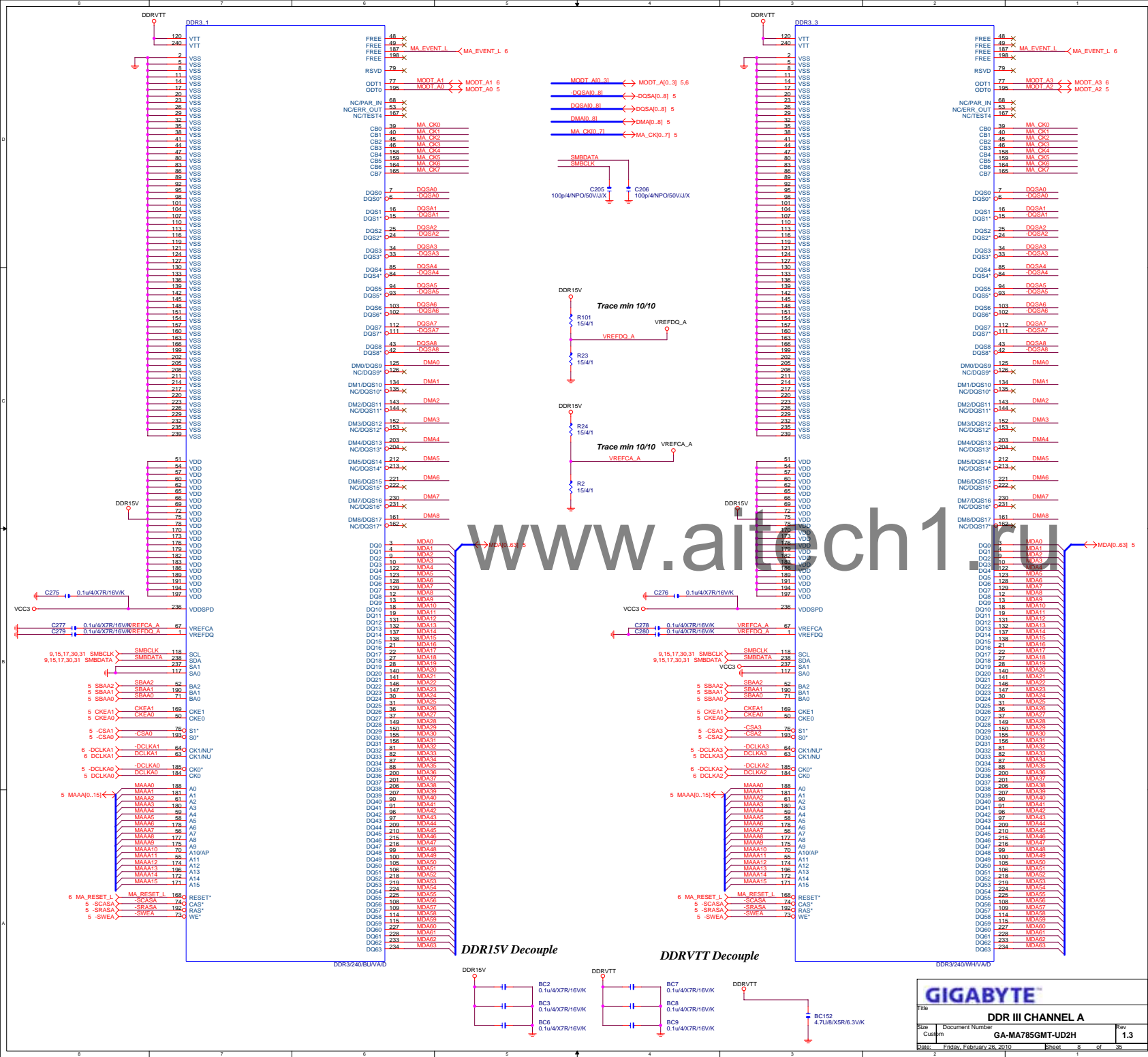
M2CPU

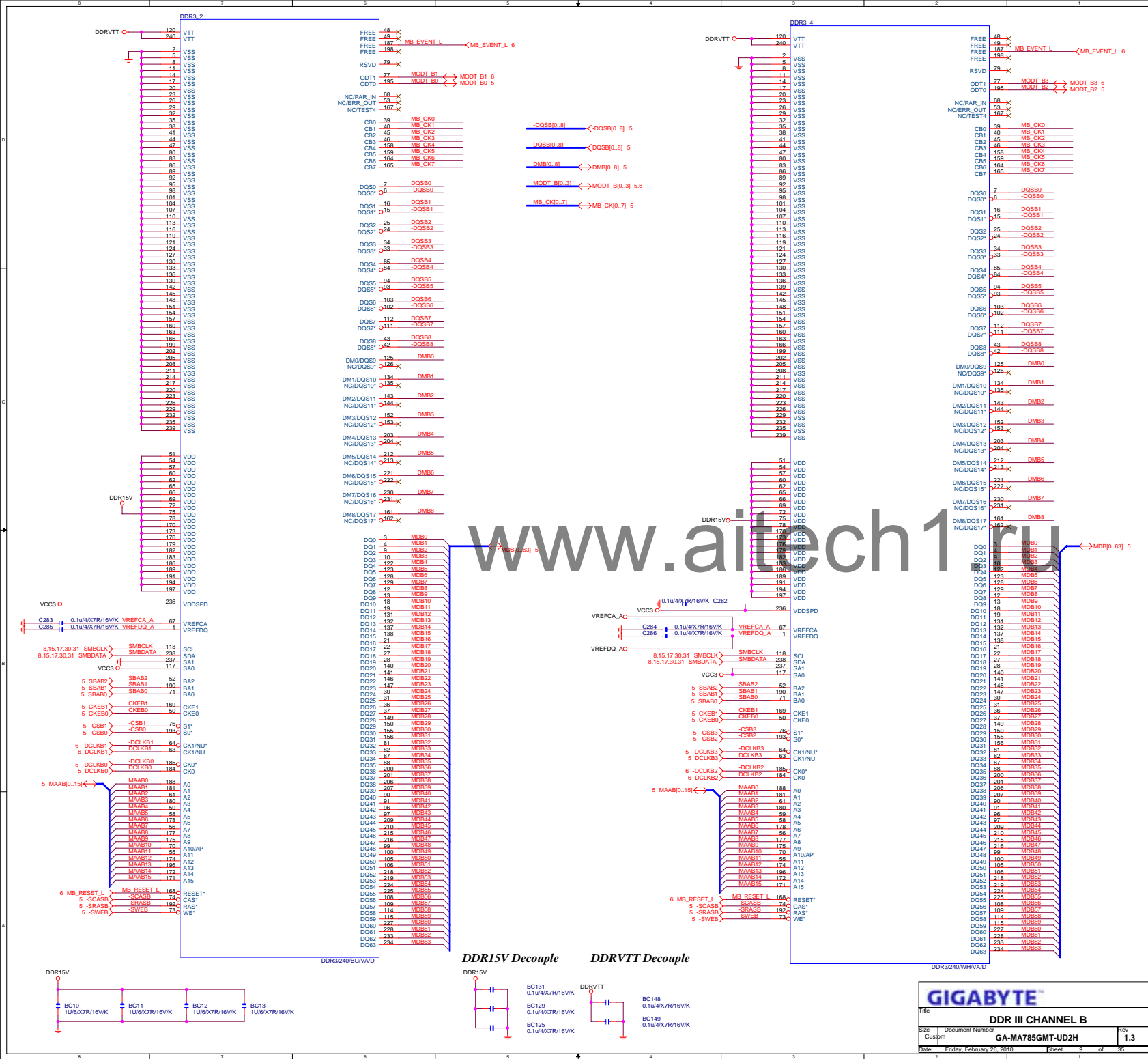
AM2RM/PP/BU/PB[12KRC-04K812-11R]



GIGABYTE®			
Title CPU HYPER TRANSPORT			
Size Custom	Document Number GA-MA785GMT-UD2H	Rev 1.3	
Date: Friday, February 26, 2010	Sheet 4	of 35	







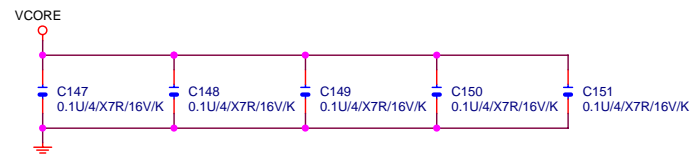
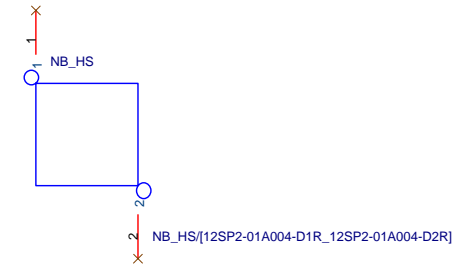


L0_CADIN_L[0..15] 4

L0_CADIN_H[0..15] 4

L0_CADOUT_L[0..15] 4

L0_CADOUT_H[0..15] 4



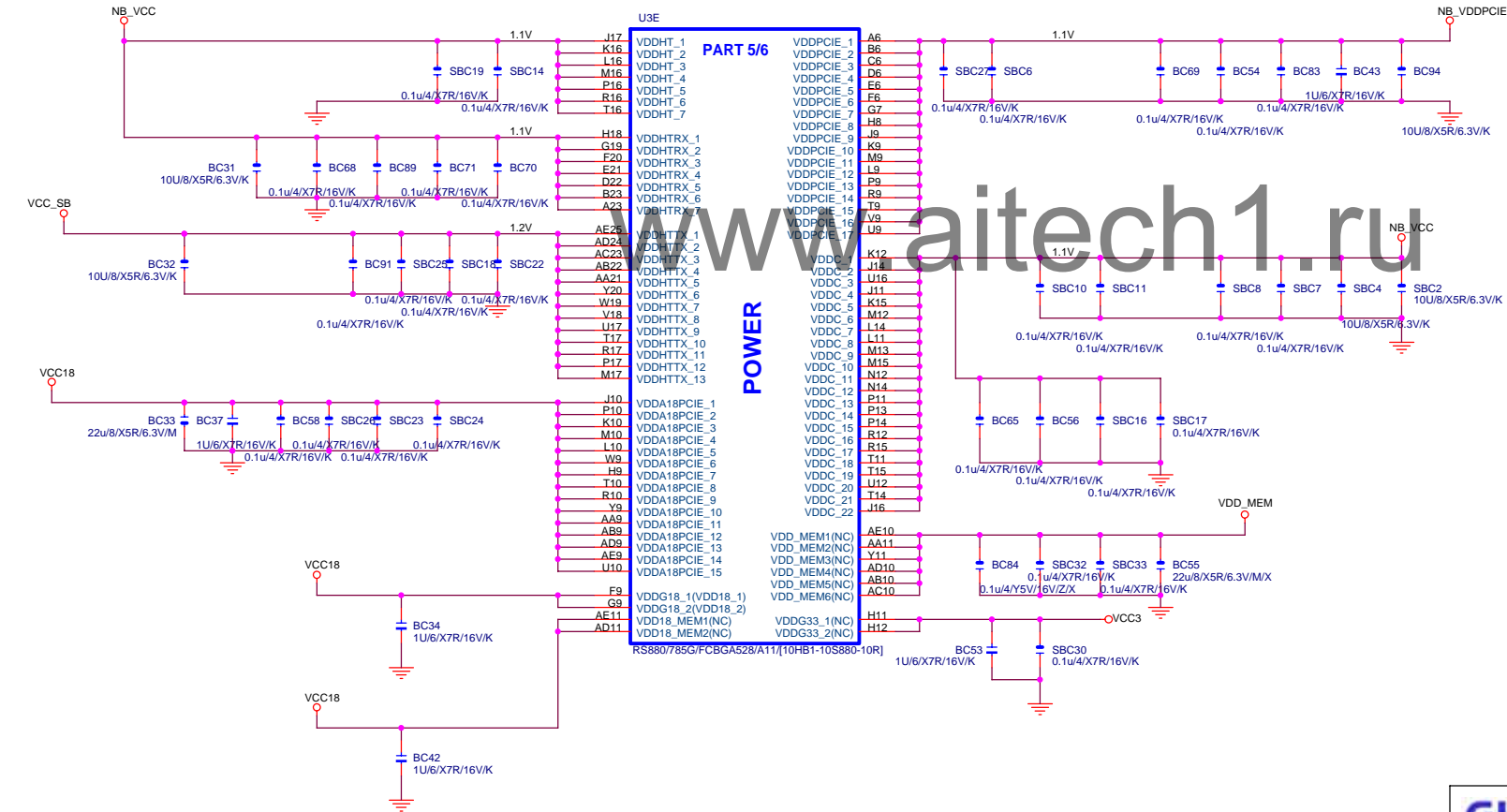
HT Link Stitching Caps

GIGABYTE™		
Title RS880 HT-LINK I/F		
Size B	Document Number GA-MA785GMT-UD2H	Rev 1.3
Date:	Friday, February 26, 2010	Sheet 10 of 35



Rev

Please use 1mm pad size,
place all ELT test pads
on bottom side only



RS740/RX780/RS780 POWER DIFFERENCE TABLE

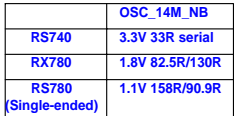
PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC

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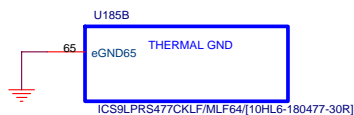
Title RS880 POWER & GND			
Size Custom	Document Number GA-MA785GMT-UD2H	Rev 1.3	
Date: Friday, February 26, 2010	Sheet 14	of 35	



- Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK



NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

GIGABYTE™

Title
ICS9LPRS477

Size	Document Number
Custom	GA-MA785GMT-UD2H

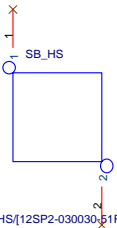
Rev	1.3
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Date: Friday, February 26, 2010 Sheet 15 of 35

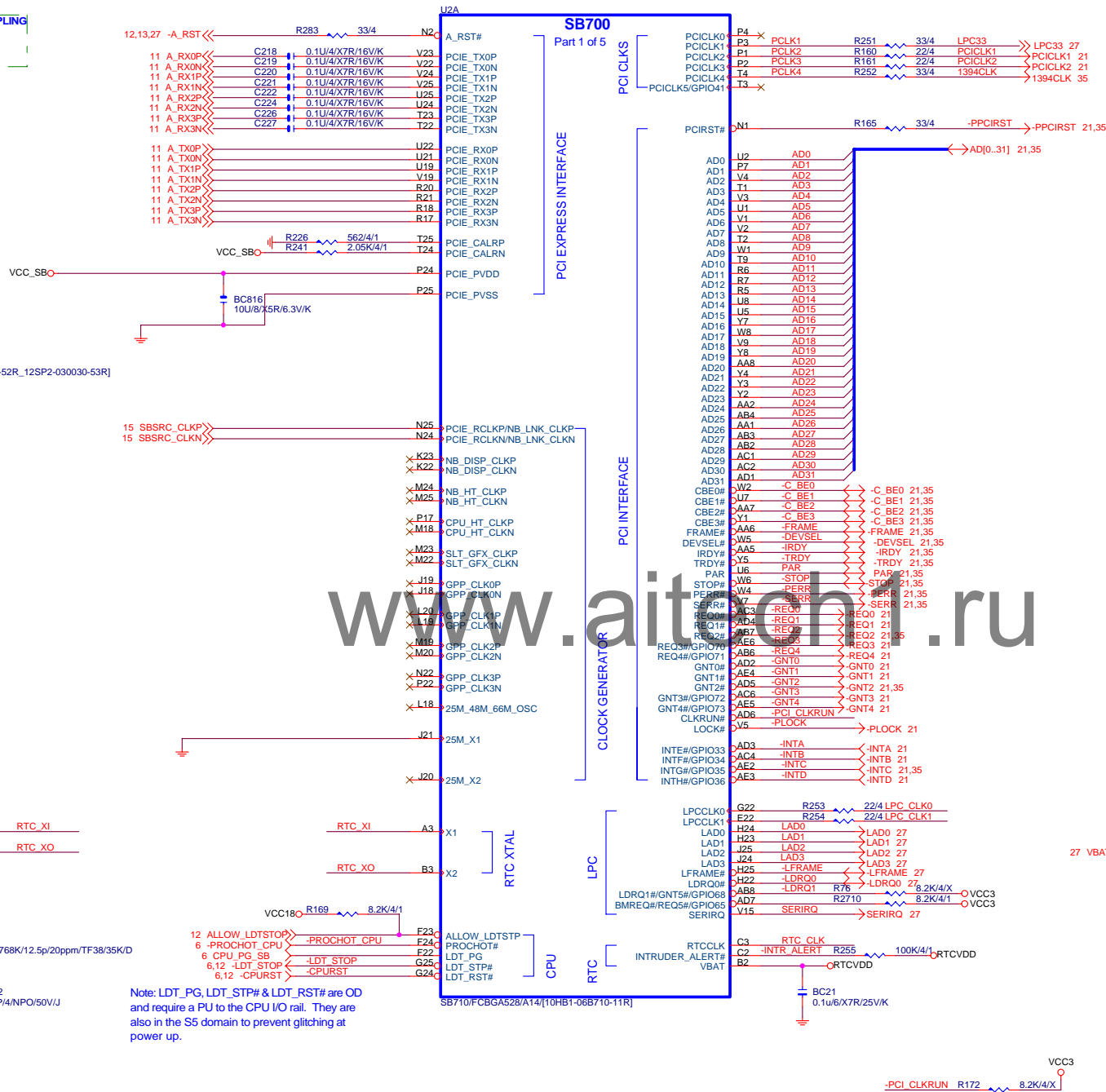


PLACE THESE PCIE AC COUPLING
CAPS CLOSE TO U600

S.B HEATSINK



SB_HS[12SP2-030030-52R_12SP2-030030-53R]



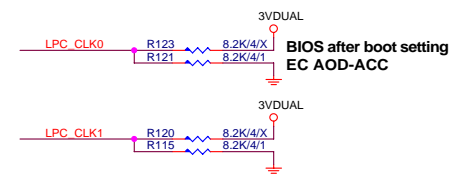
Note: LDT_PG, LDT_STP# & LDT_RST# are OD
and require a PU to the CPU I/O rail. They are
also in the S5 domain to prevent glitching at
power up.

PULL HIGH
WATCHDOG TIMER
ON NB_PWRGD
ENABLED

PULL LOW
WATCHDOG TIMER
ON NB_PWRGD
DISABLED
DEFAULT

PCLK2
USE
DEBUG
STRAPS

PCLK3
IGNORE
DEBUG
STRAPS
DEFAULT



LPC_CLK0
Rev.A12

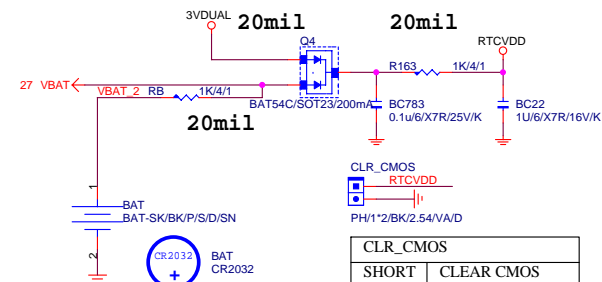
LPC_CLK1

PULL HIGH
IMC
ENABLED
AOD Extreme

PULL LOW
IMC
DISABLED
DEFAULT

CLKGEN
ENABLED

CLKGEN
DISABLED
DEFAULT

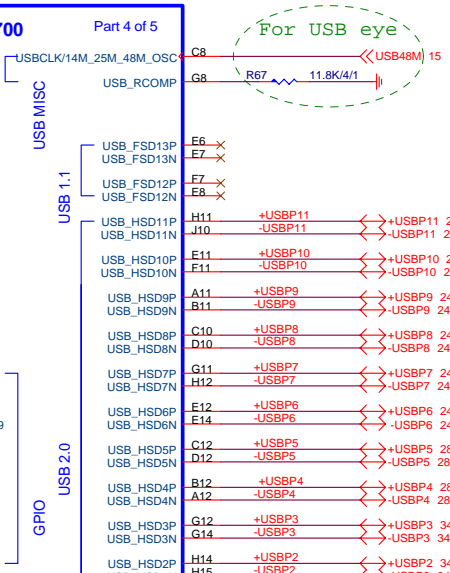
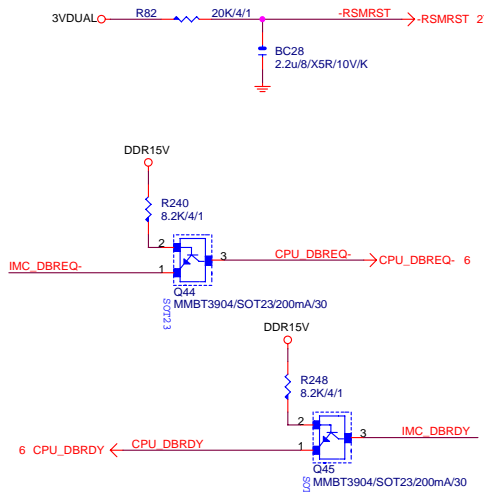
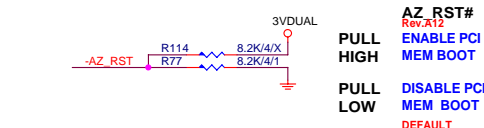
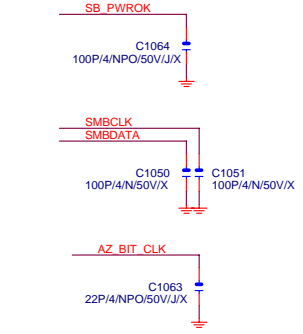
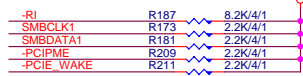
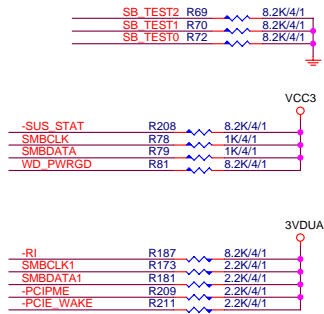


CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

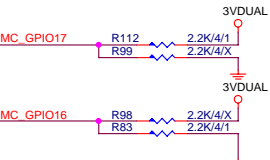
GIGABYTE

Title ATI SB710 PCIE/PCI/CPU/LPC		
Size Custom	Document Number GA-MA785GMT-UD2H	Rev 1.3
Date Friday, February 26, 2010	Sheet 16	of 35

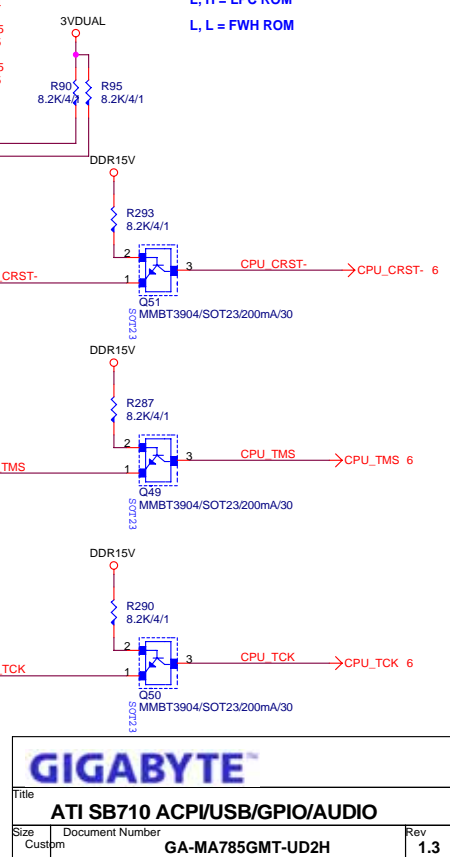


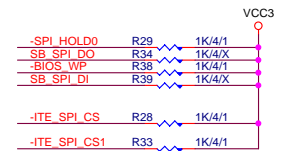
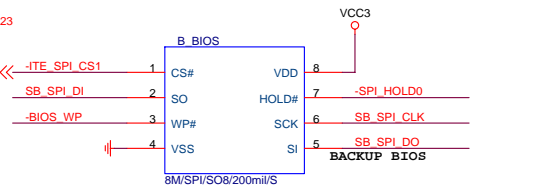
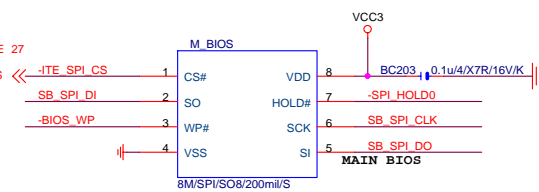
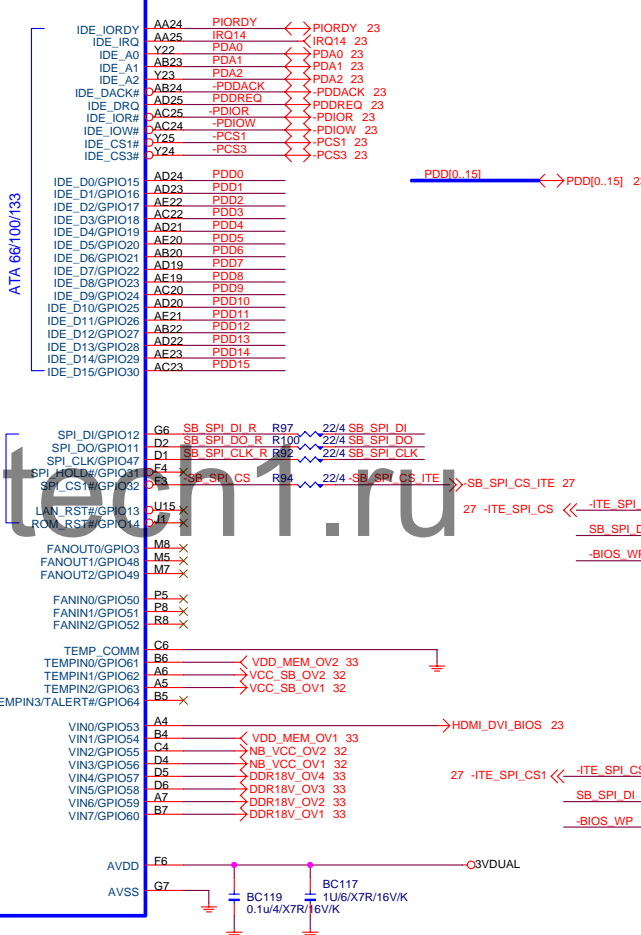
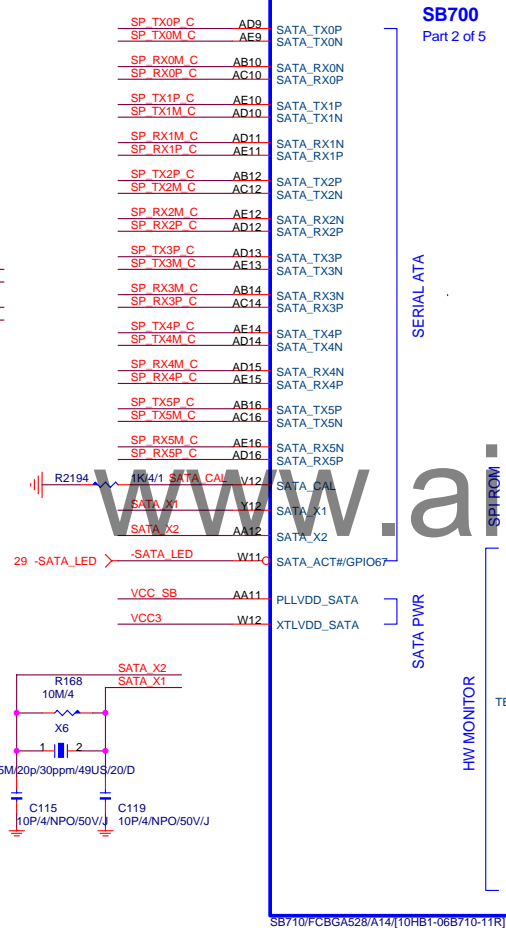
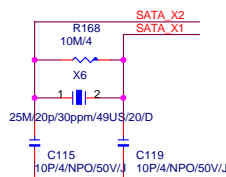
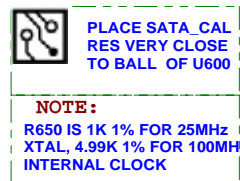
USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

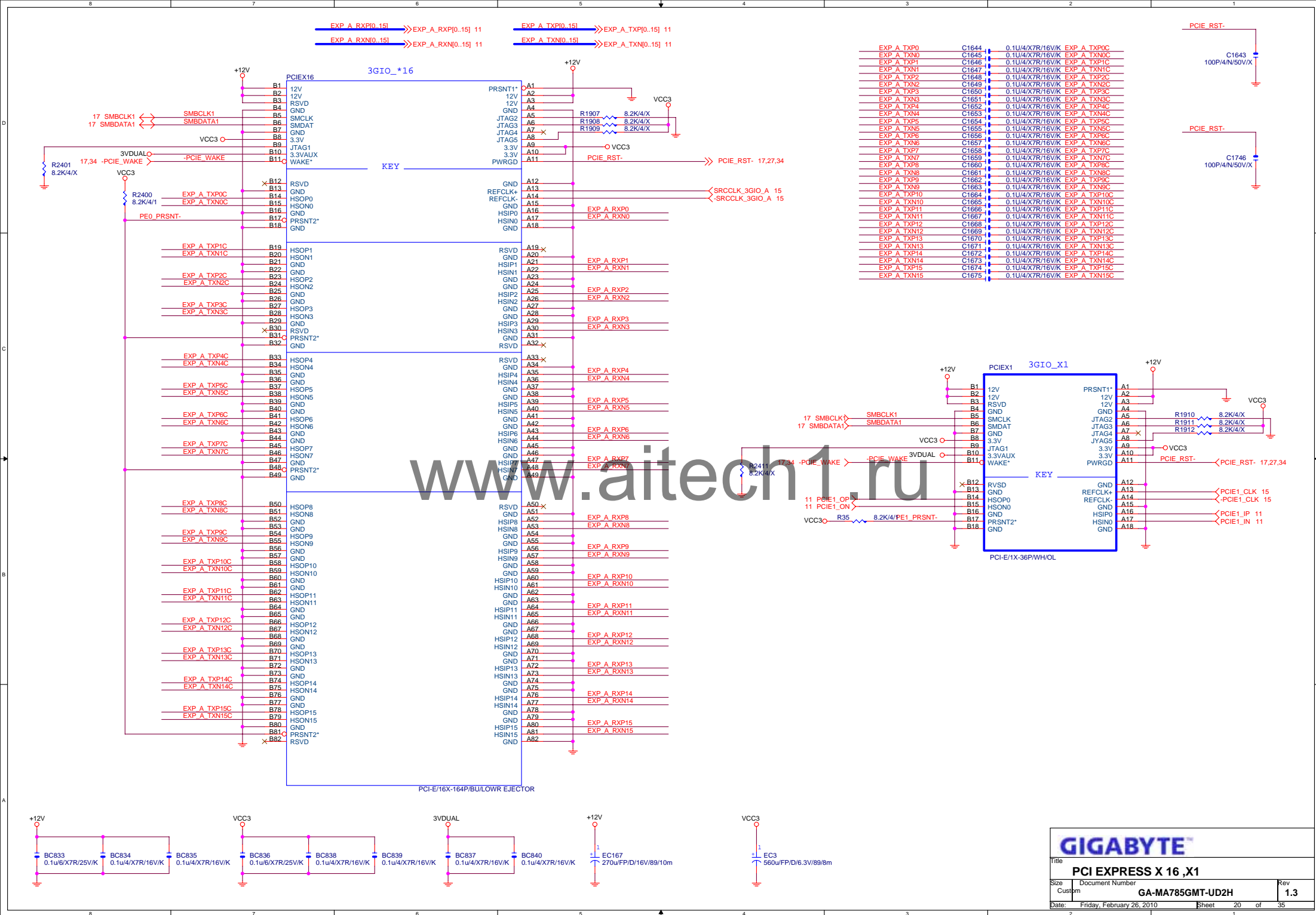
either HWM inputs or PWR_GD signals can be used for power-up sequencer



IMC_GPIO17 IMC_GPIO16
ROM TYPE:
H, H = Reserved
H, L = SPI ROM DEFAULT
L, H = LPC ROM
L, L = FWB ROM

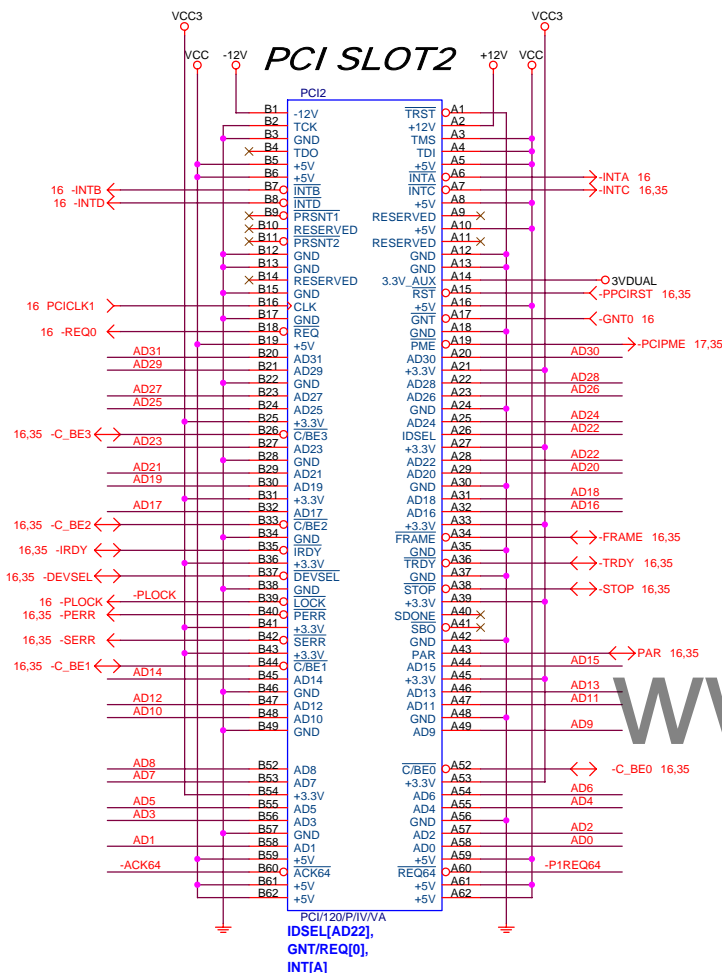




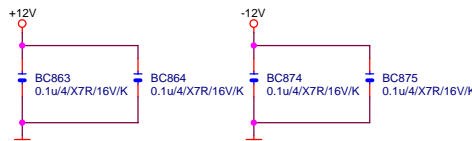
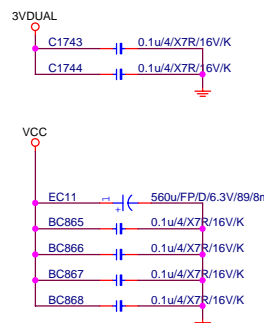
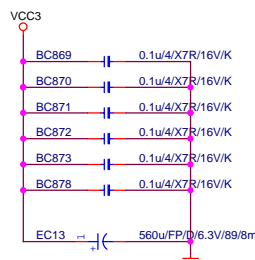
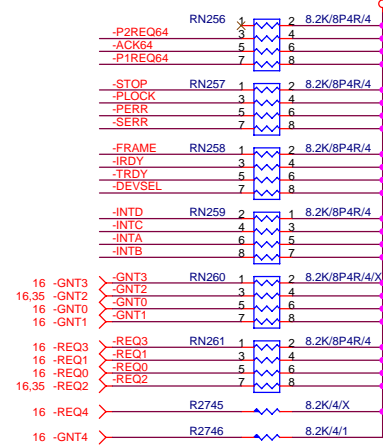
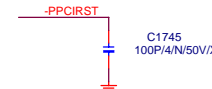
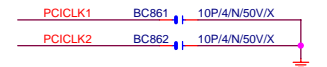
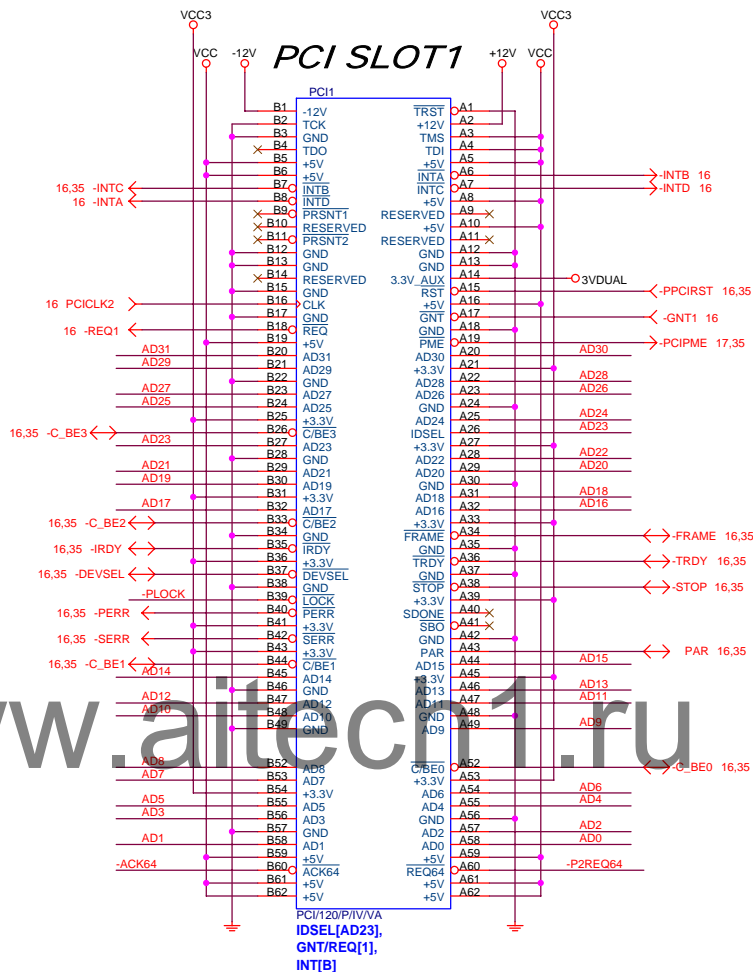


PCI SLOT 1,2

16,35 AD[0..31] ↔ AD[0..31]

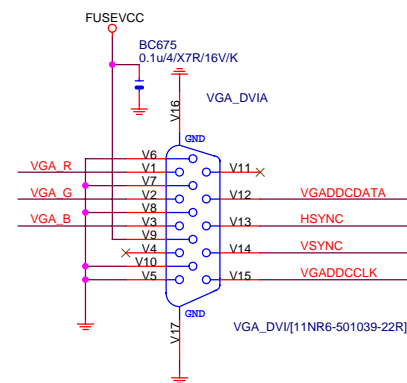
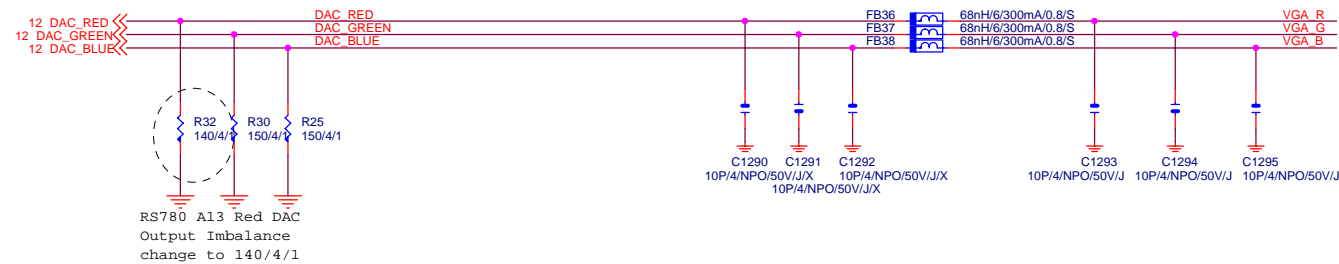
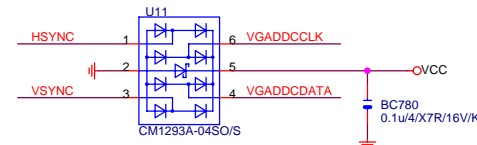
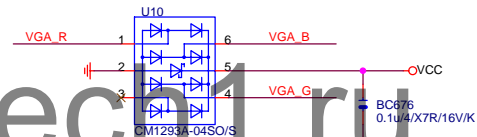
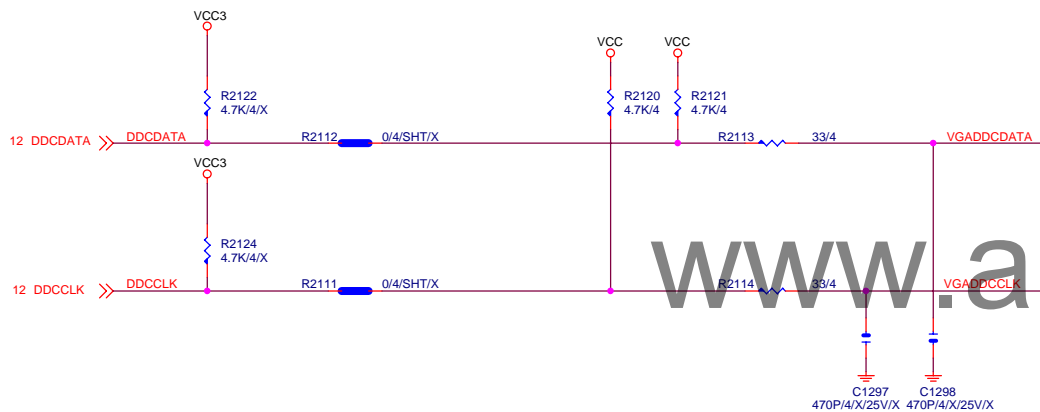
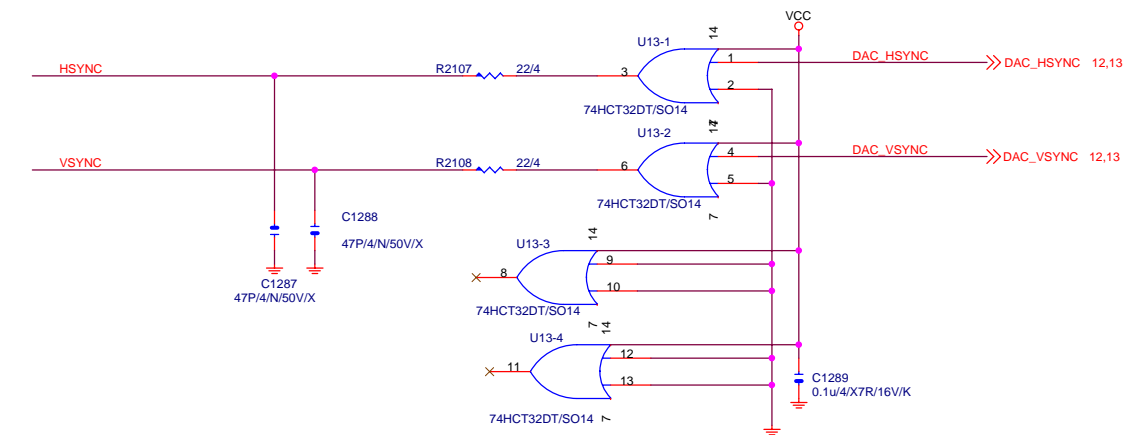


PCI SLOT1



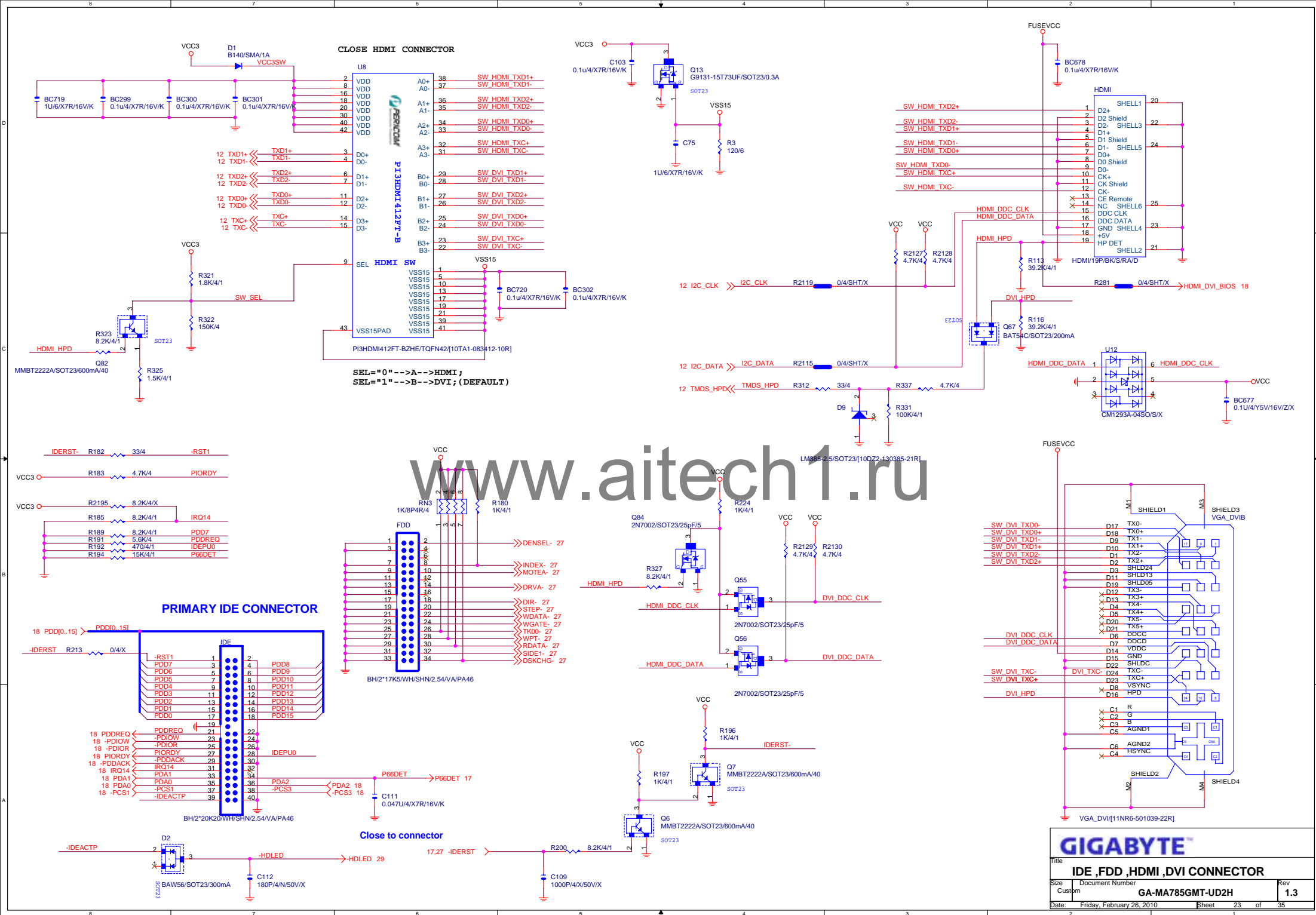
GIGABYTE

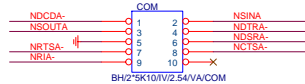
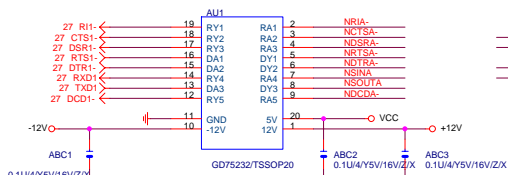
Title			PCI SLOT 1,2
Size	Document Number	Rev	
Custom	GA-MA785GMT-UD2H	1.3	
Date:	Friday, February 26, 2010	Sheet	21 of 35



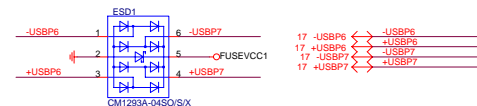
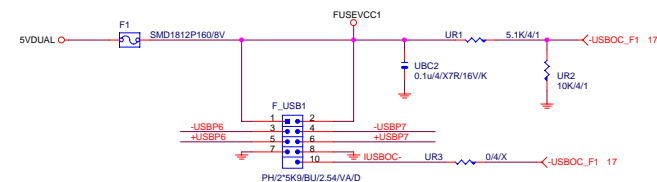
GIGABYTE

Title		
RGB		
Size	Document Number	Rev
Custpm	GA-MA785GMT-UD2H	1.3
Date:	Friday, February 26, 2010	Sheet 22 of 35

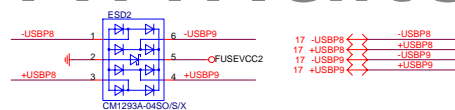
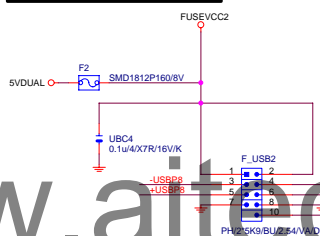




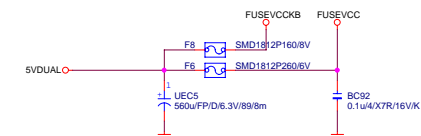
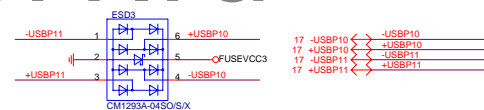
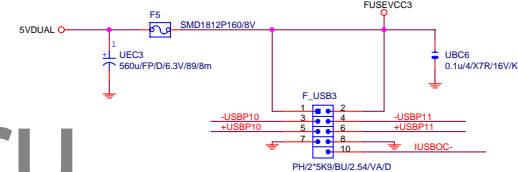
FRONT SIDE USB1



FRONT SIDE USB2



FRONT SIDE USB3



GIGABYTE

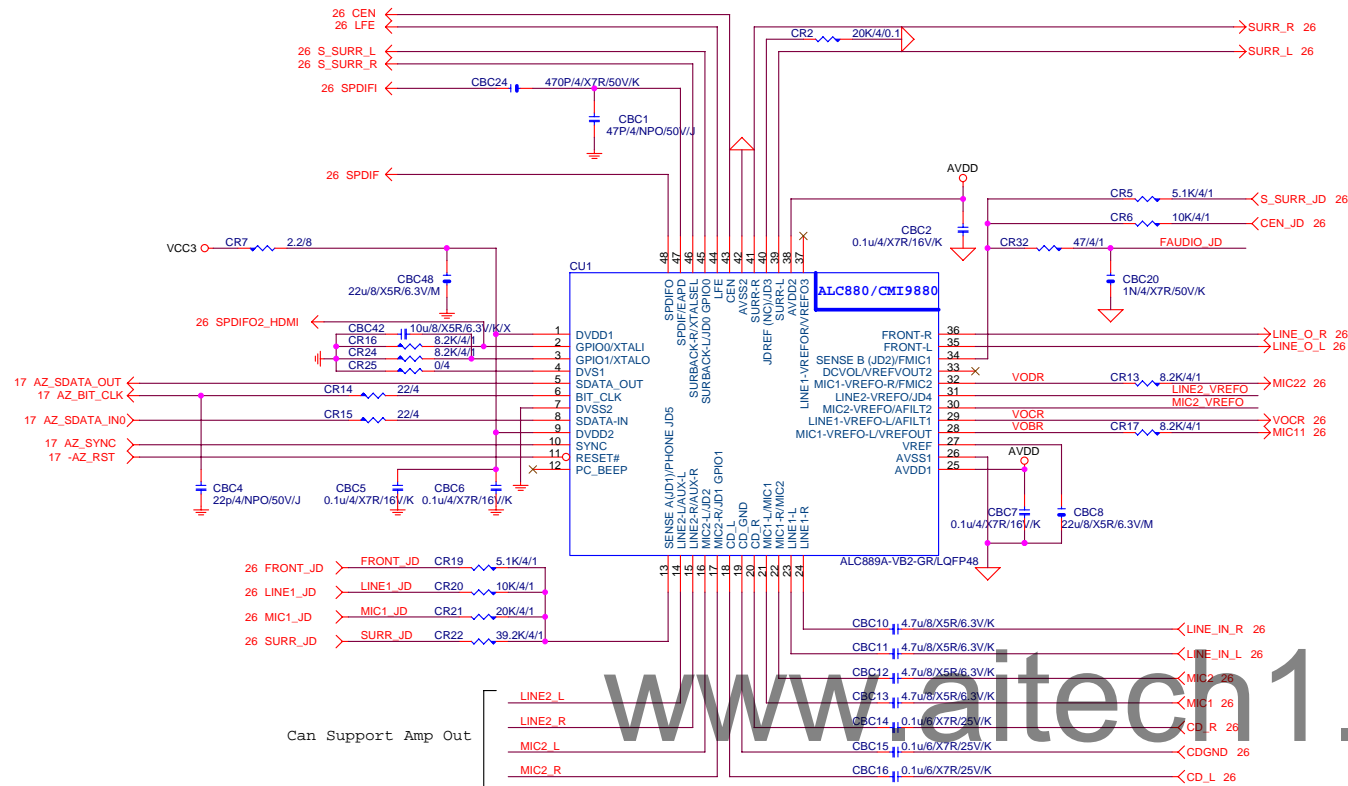
COM/LPT/F_USB

Document Number GA-MA785GMT-UD2H

Date Friday, February 26, 2010

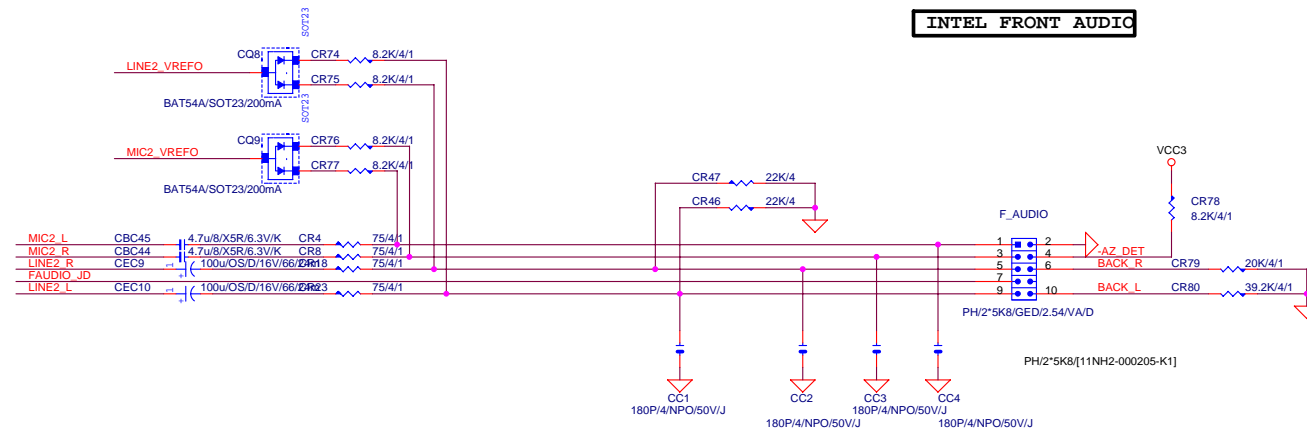
Sheet 24 of 35

Rev 1.3



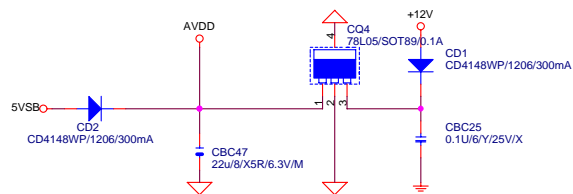
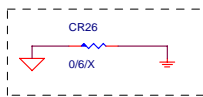
AZALIA CODEC ALC892/ALC889A/ Colay

	ALC892		ALC889A
CR16	X		O
CR24	X		O
CR25	X		O
CBC42	10uF/X5R		X
CR2	20K/1%		20K/0.1%
CR9	O		X
CR10	X		O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R		4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR28/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm		75 ohm

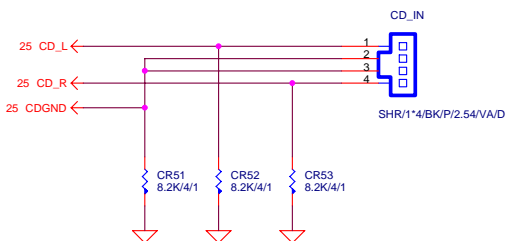


GIGABYTE

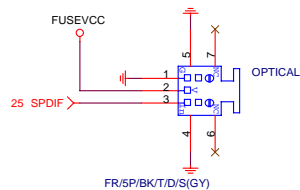
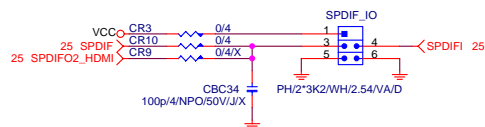
Title	ALC889A CODEC		
Size	Document Number	Rev	
Custom	GA-MA785GMT-UD2H	1.3	
Date:	Friday, February 26, 2010	Sheet	25 of 35



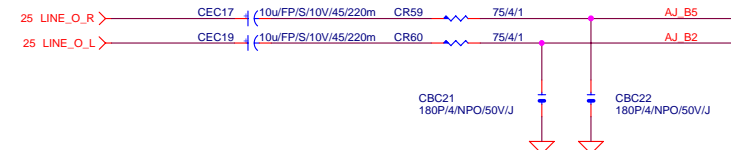
CD IN



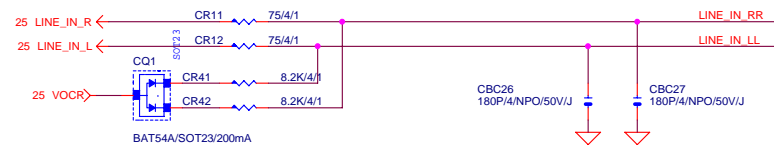
SPDIF



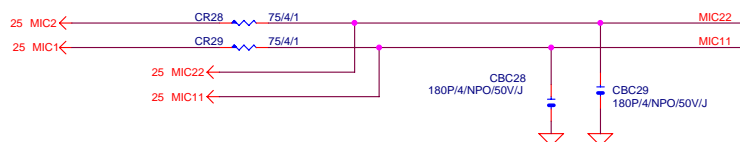
LINE OUT FRONT OUT



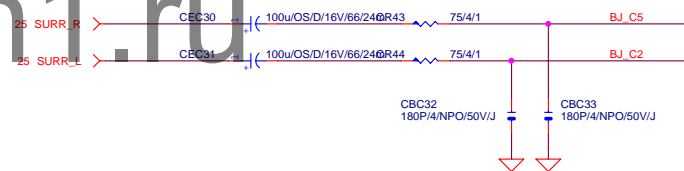
LINE-IN



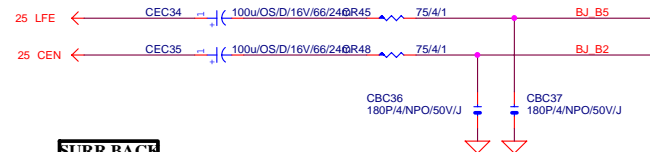
MIC



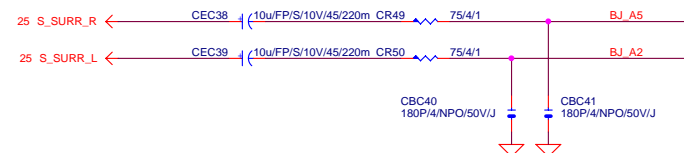
SURROUND



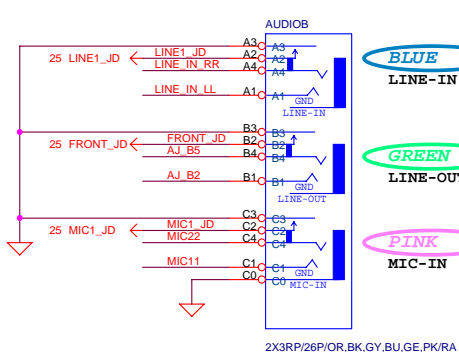
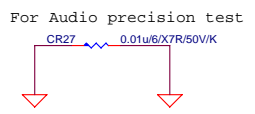
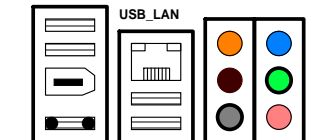
CEN/LFE



SURR BACK



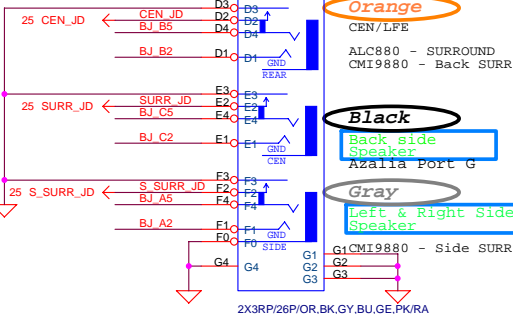
USB_1394_ESATA



BLUE
LINE-IN

GREEN
LINE-OUT

PINK
MIC-IN



Orange
CEN/LFE

Black
Back side
Speaker

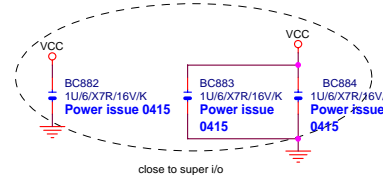
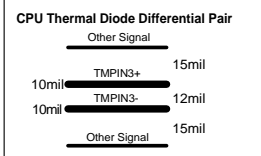
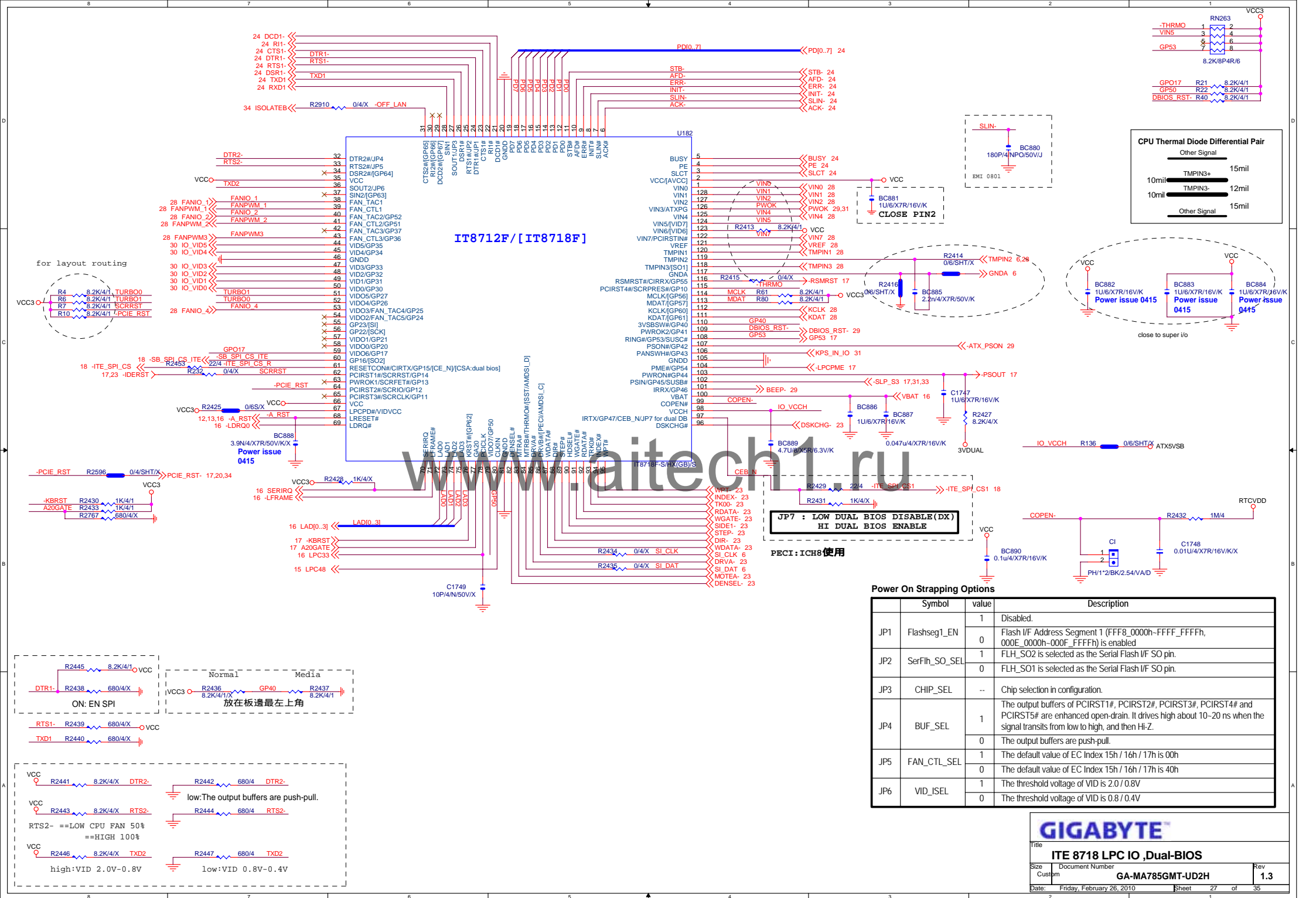
Gray
Left & Right Side
Speaker

A3R7/13P/B/[11NR6-403006-01_11NR6-403006-02]
3R7+15P/[11NR6-403004-11]

A3R7/13P/0BG/[11NR6-403006-71]
3R7+15P/[11NR6-403004-31]

GIGABYTE

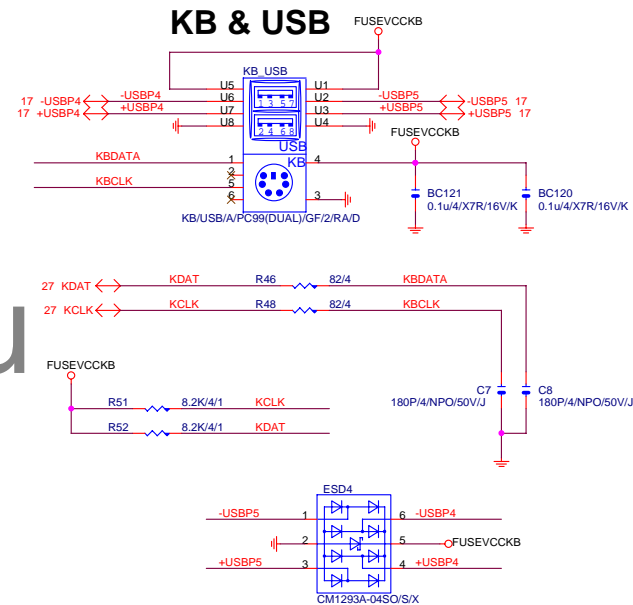
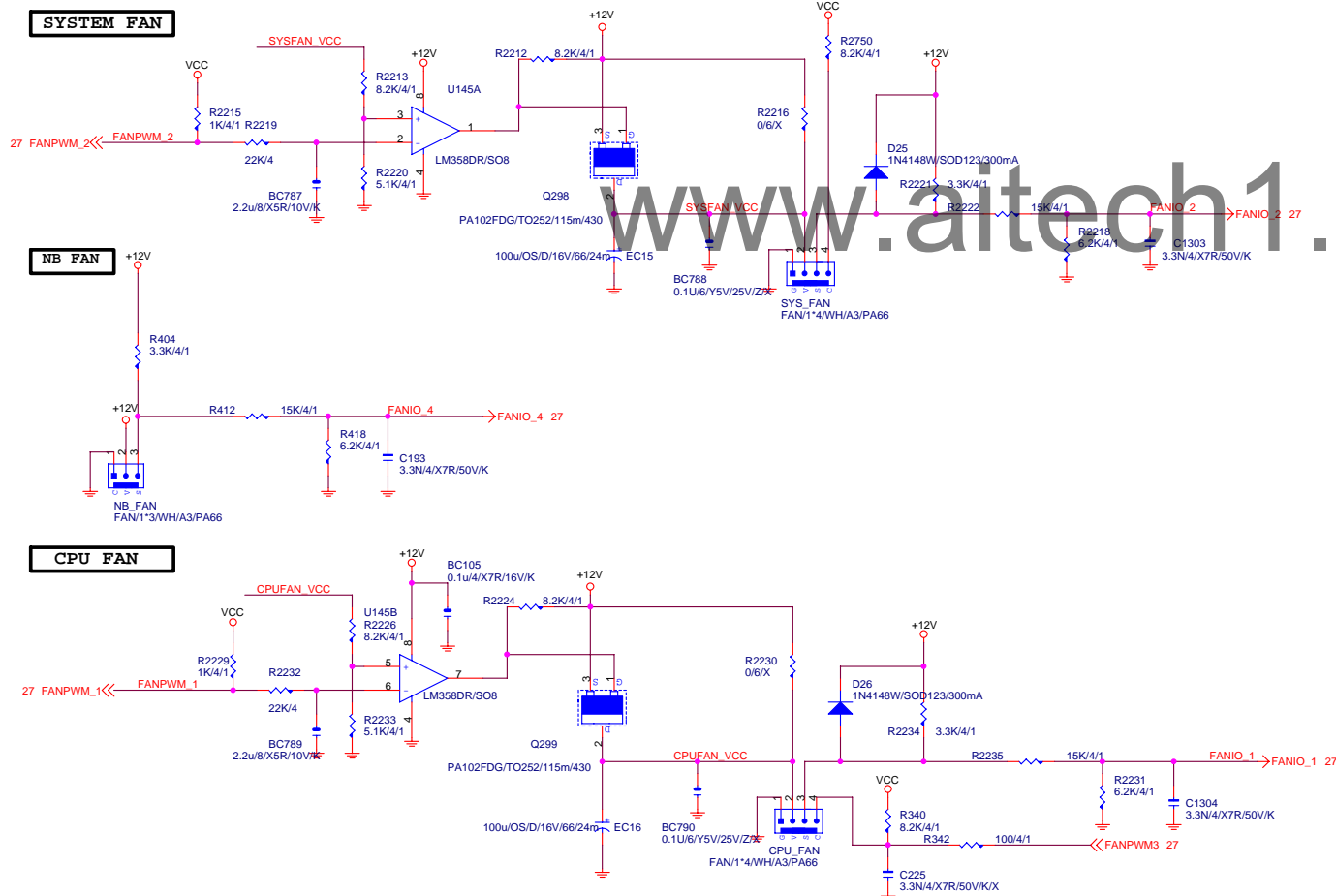
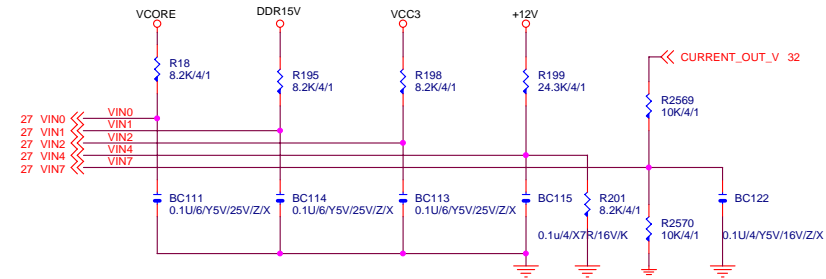
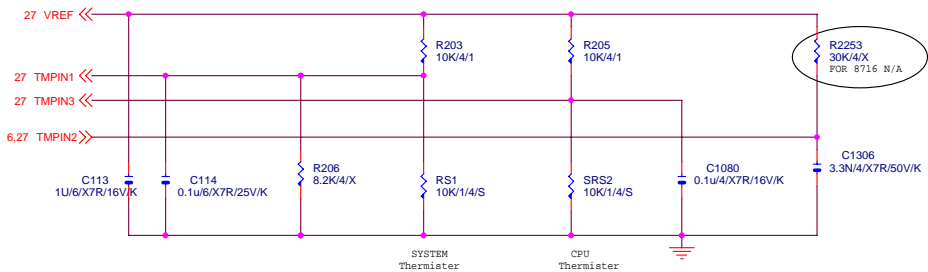
Title		
AUDIO JACK		
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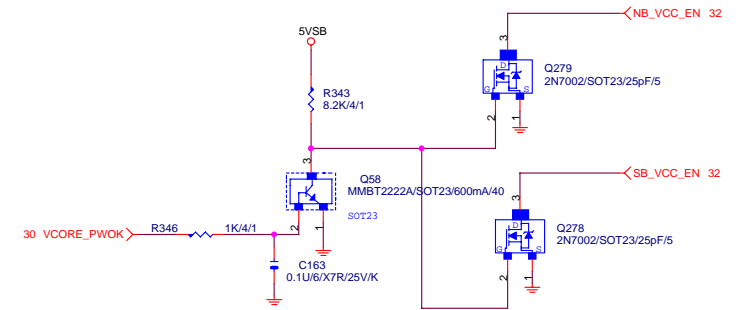
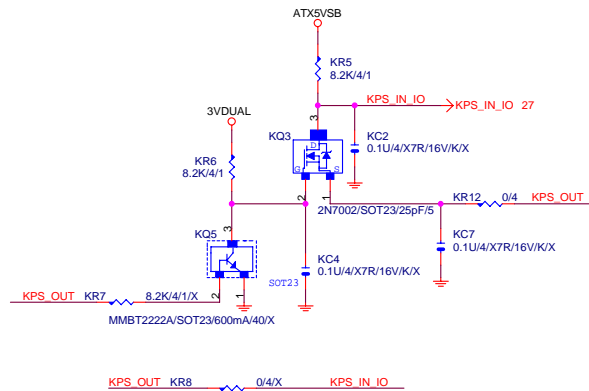
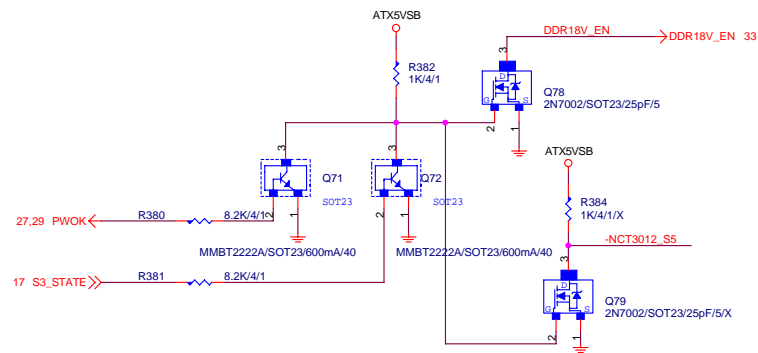
Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h-FFFF_FFFFh, 000E_0000h-000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_S01 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10-20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

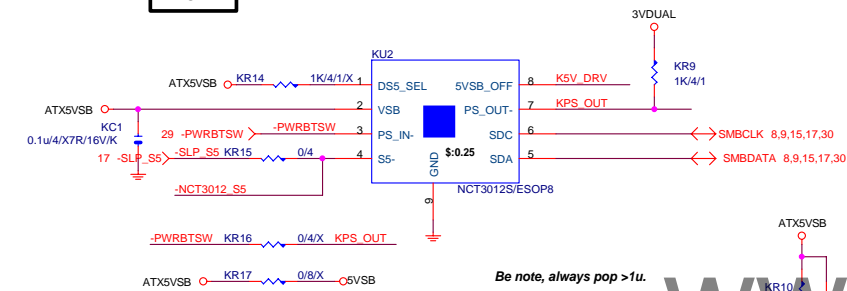
Hardware Monitor circuits



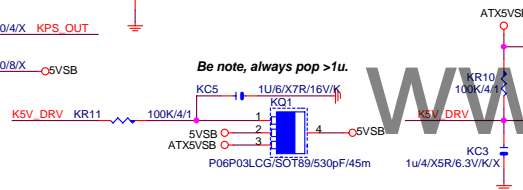
1



EUP

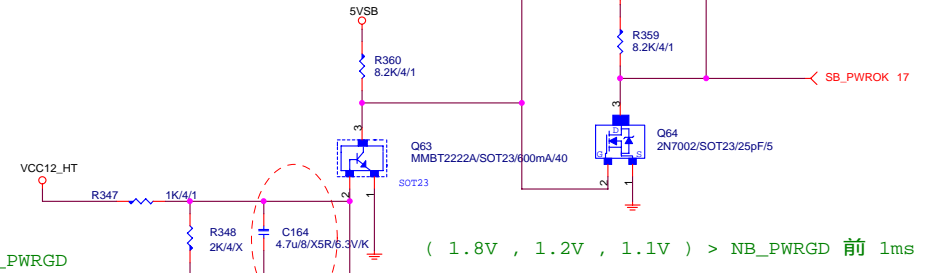


Function Selection. Strapped by VSB
 I Strapped to high :
 DeepS5_Sel = 1:
 System will enter the deep S5 state after 6 sec
 delays when AC power on.
 I Strapped to low : (Default)
 DeepS5_Sel = 0:
 System will not enter the deep S5 state when AC
 power on. System is in normal ACPI S5 state.



Be note, always pop >1u.

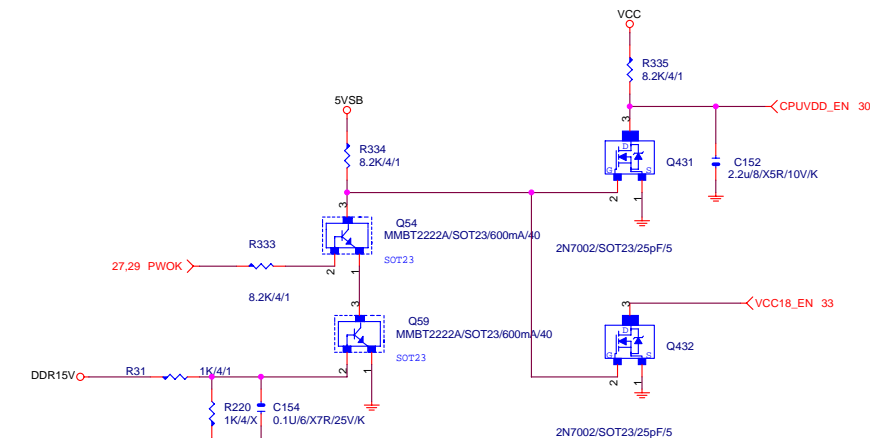
www.aitech1.ru



PWOK > NB_PWRGD / SB_PWRGD

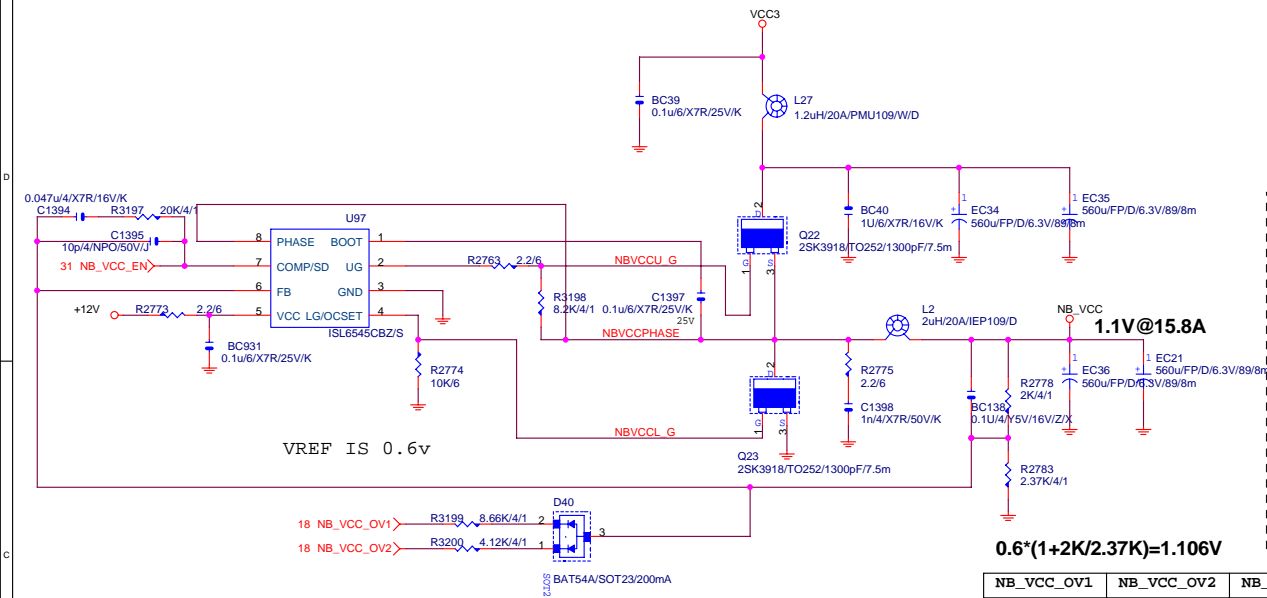
(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms

For ACC Function

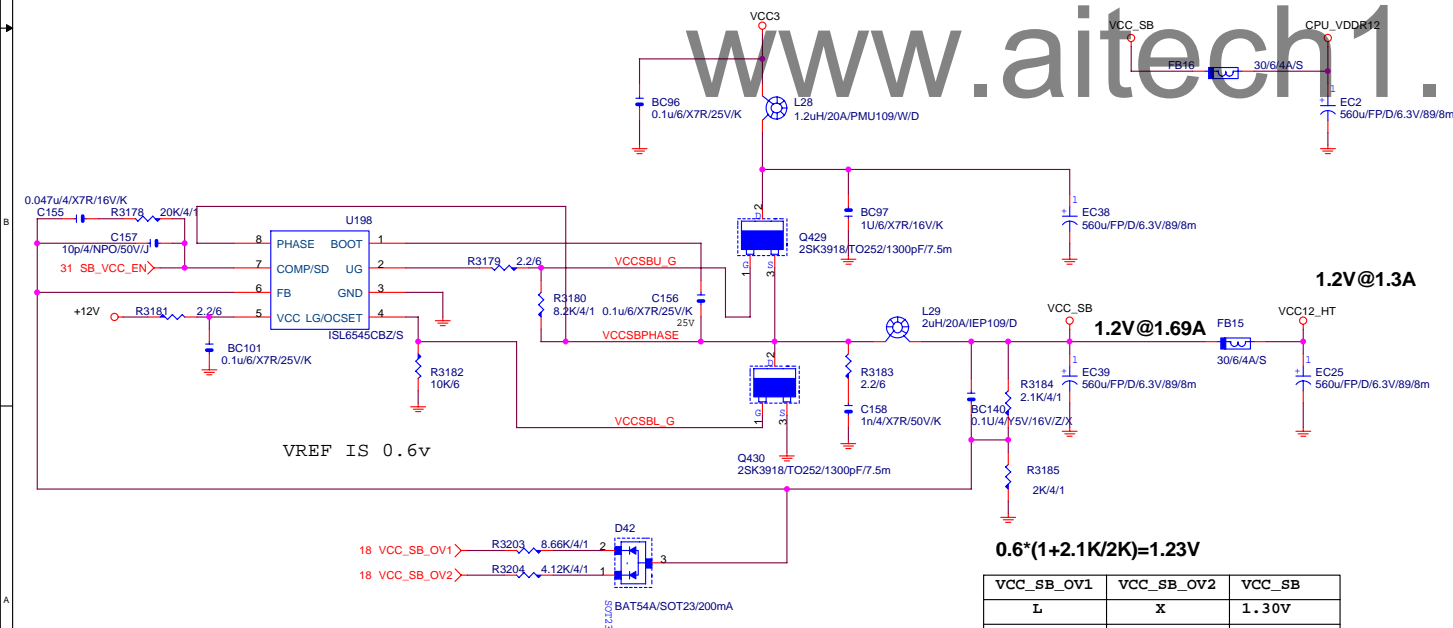
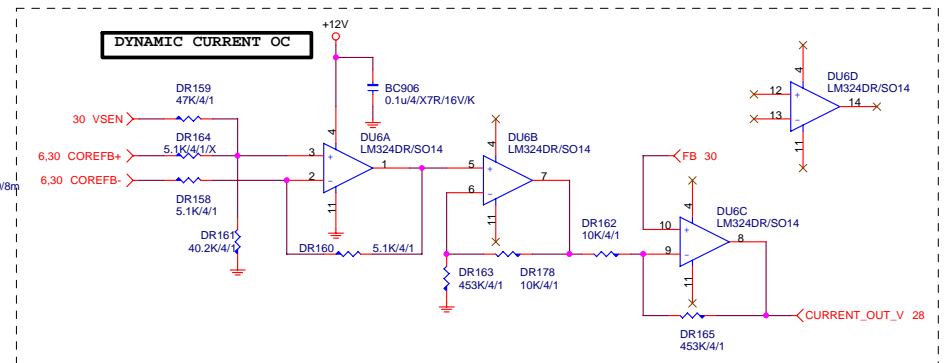


GIGABYTE

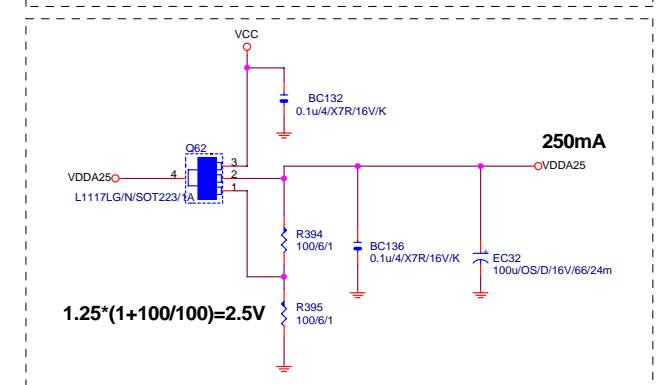
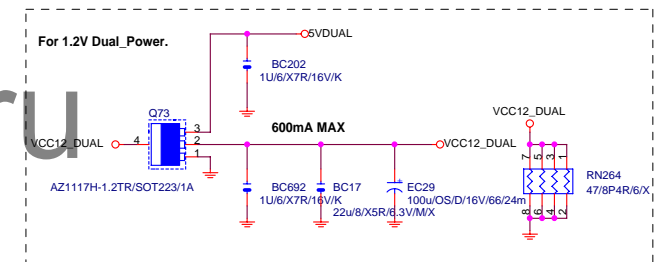
POWER SEQUENCE ,EUP			
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NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V

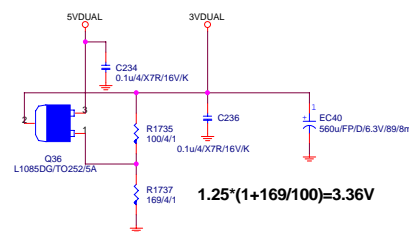


VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V

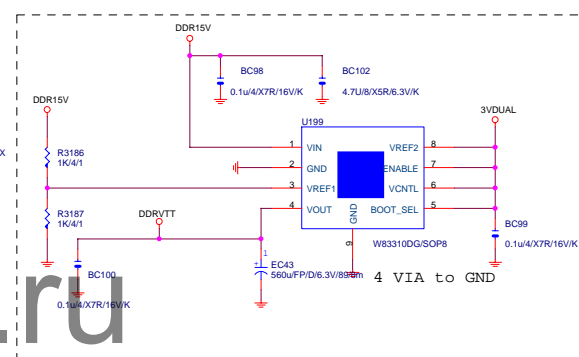


GIGABYTE

3VDUAL

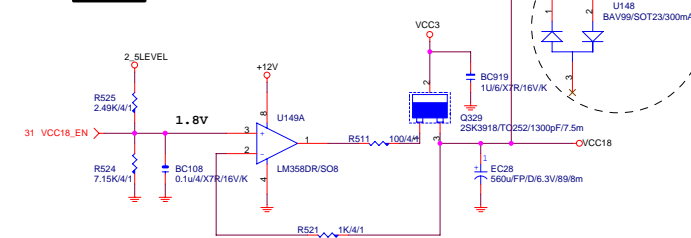
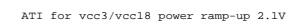


$$1.25 \times (1 + 169/100) = 3.36V$$



4 VIA to GNI

VDD_MEM_OV1	VDD_MEM_OV2	VDD_MEM
L	X	1.60V
X	L	1.70V
L	L	1.80V



$$0.6 \cdot (1 + 1.69K/1K) = 1.614V$$

DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
L	X	X	X	1.65V
X	L	X	X	1.70V
L	L	X	X	1.75V
X	X	L	X	1.80V
L	X	L	X	1.85V
X	L	L	X	1.90V
L	L	L	X	1.95V

DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
X	X	X	L	2.00V
L	X	X	L	2.05V
X	L	X	L	2.10V
L	L	X	L	2.15V
X	X	L	L	2.20V
L	X	L	L	2.25V
X	L	L	L	2.30V
L	L	L	L	2.35V

GIGABYTE™

DDRII POWER , VCC18

GA-MA785GMT-UD2H

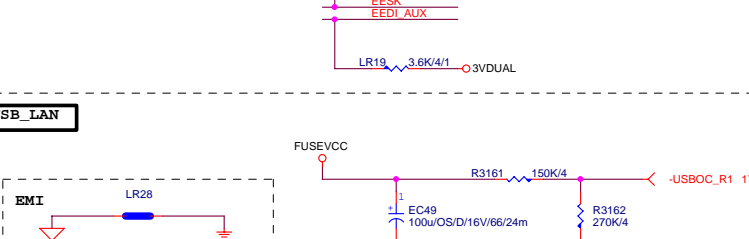
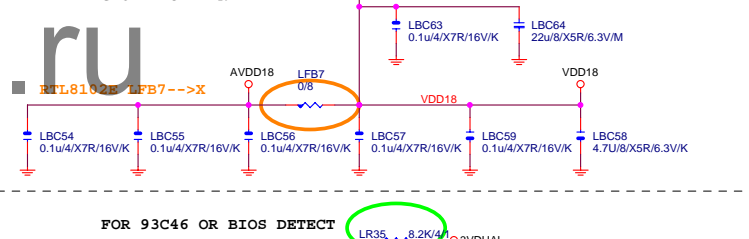
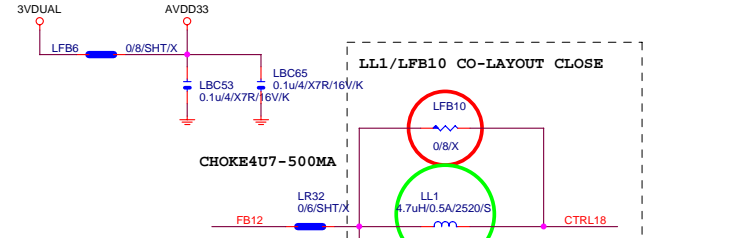
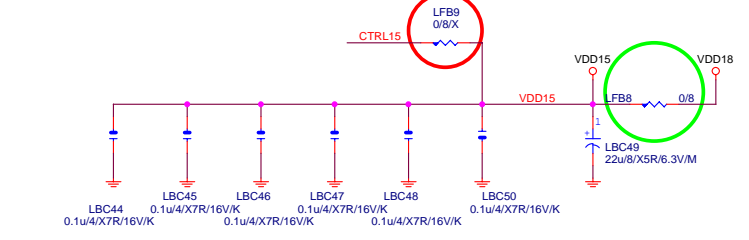
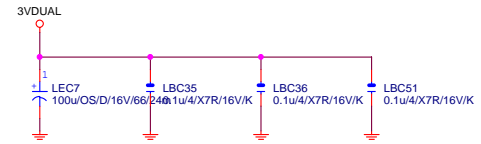
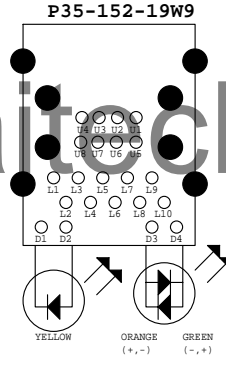
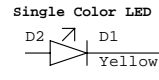
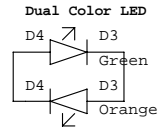
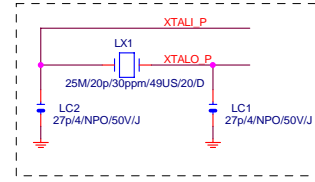
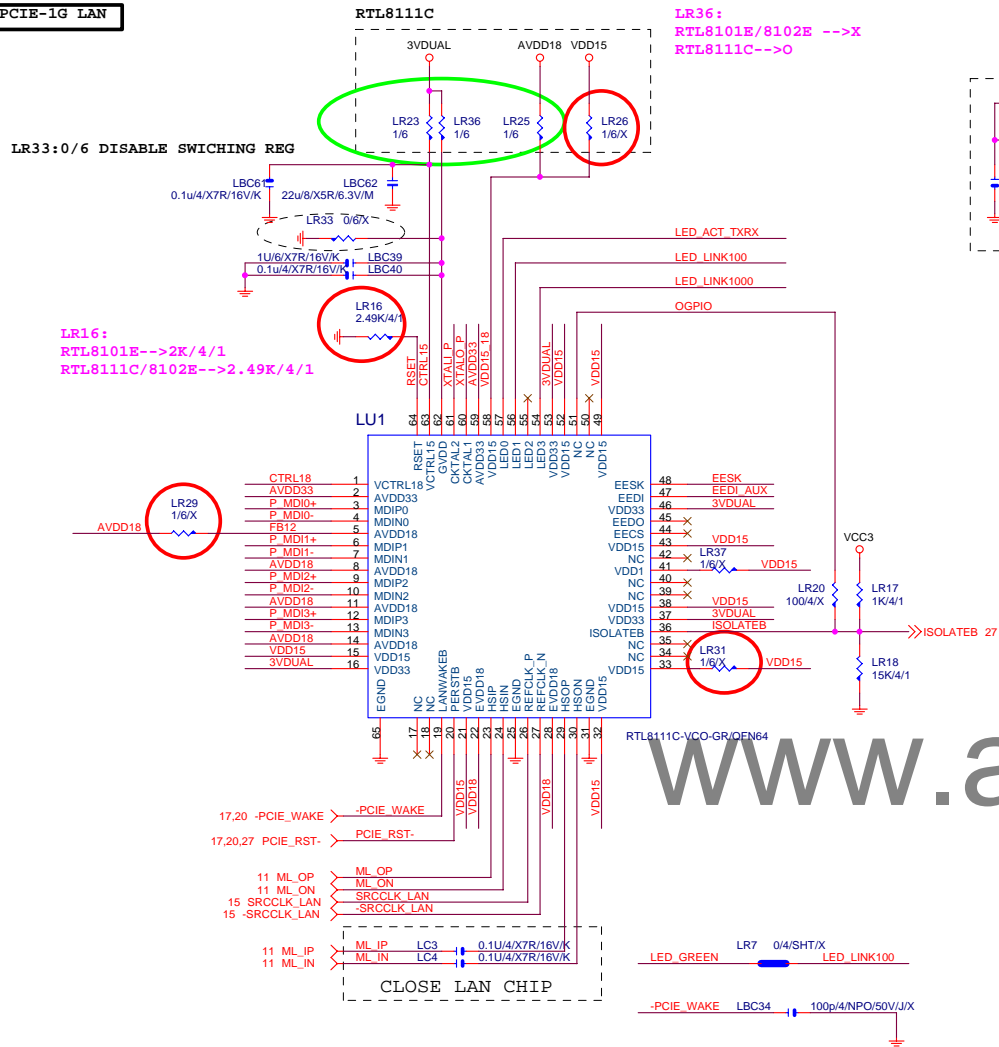
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PCIE-1G LAN

LR33:0/6 DISABLE SWITCHING REG

LR16:
RTL8101E-->2K/4/1
RTL8111C/8102E-->2.49K/4/1

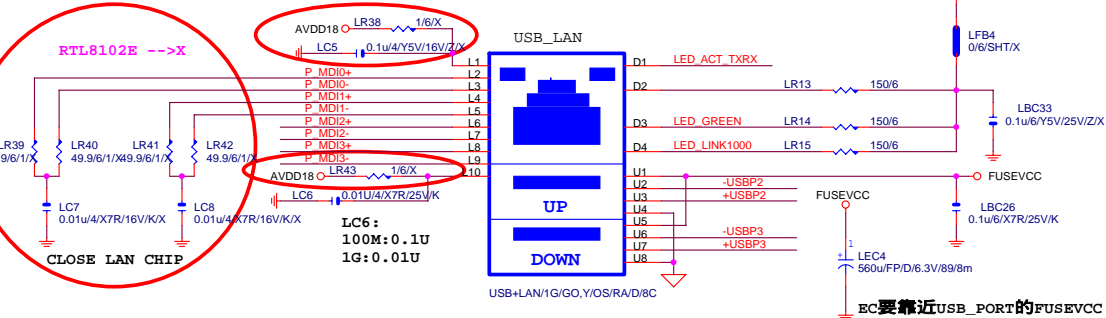


USB_LAN CONNECTOR

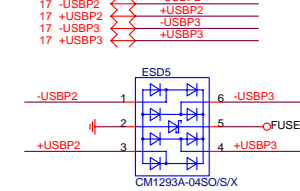
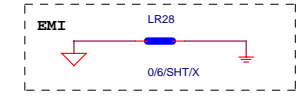
RTL8101E:LR38/LC5/LR43/LC6-->0
RTL8102E:LC5/LC6-->0
RTL8111C:LC6-->0

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)

1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1



USB_LAN



GIGABYTE		
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